IN THE SPECIFICATION:

Please amend the paragraph beginning on page 2, line 17 as follows:

In some cases it is advantageous to downsample a signal. For example, with images, it is often advantageous to view an image in a smaller frame. However, the algorithms for generating a downsampled signal vs. a non-downsampled signal will typically vary significantly. Thus, typically it is required to provide separate hardware structures to generate either a downsampled signal or a non-downsampled signal. This is highly disadvantageous as it results in increased hardware area, complexity and cost. Thus, it would be advantageous to develop a hardware structure capable of operating in one of a downsampling or non-downsampling modes, while reducing the redundancy of hardware elements as much as possible.

Please amend the Abstract (page 27) as follows:

~~The present invention provides an~~ An algorithm and hardware structure is described for numerical operations on signals that is reconfigurable to operate in a downsampling or non-downsampling mode. According to one embodiment, a plurality of adders and multipliers are reconfigurable via a switching fabric to operate as a plurality of MAAC (multiply-add-accumulator) kernels (described in detail below), when operating in a non-downsampling mode and a plurality of MAAC kernels and AMAAC (add-multiply-add-accumulator) kernels (described in detail below), when operating in a downsampling mode.